Code No: RA320501 **RA**

**III B.Tech II Semester Regular Examinations, April/May 2005**
**ADVANCED COMPUTER ARCHITECTURE**
**(Electronics & Communication Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Distinguish between
   i. data processing
   ii. information processing
   iii. Knowledge processing
   iv. intelligence processing.
   (b) What do you understand by balancing of system bandwidth? Why is it necessary? Illustrate with suitable examples.
2. (a) Classify pipeline processors according to the levels of processing giving examples of each class.
   (b) What are reservation tables in the context of pipelines? Why are they required? Give a sample pipeline with both feedforward and feedback connections and show how a reservation table is created for it.
3. Explain the working of a Barrel Shifter with 16 nodes and give its routing functions.
4. (a) What is an associative memory? Discuss a simple associative memory organization with suitable diagrams.
   (b) Explain the architecture of PEPE association processor
5. (a) Explain briefly the communication between processors in a Multiprocessor environment.
   (b) With suitable diagram, explain loosely coupled and tightly coupled Multiprocessors.
6. (a) List the major characteristics, advantages and shortcomings of three types of multiprocessor operating systems.
   (b) List the four main sources of performance degradation of the dynamic coherence check algorithm.
7. (a) Explain the organization of a dynamic data flow computer.
   (b) What is data flow graph? Explain how a data flow graph constructed.
8. (a) Give the features of Hydra operating system.
   (b) Demonstrate the effect of memory contention on the performance of C.mmp.

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